20. (currently amended)An electronic system comprising:

A. a ~~first~~ functional circuit having a mode input lead receiving a mode signal to place the ~~first~~ functional circuit in one of a ~~first~~ functional mode in which the functional circuit operates normally and ~~second~~ a test mode in which at least part of the functional circuit is disabled; and

B. a ~~second~~ selector circuit having a mode output lead connected to the mode input lead of the ~~first~~ functional circuit and having ~~first and second~~ a pair of clock leads separate from the ~~first~~ functional circuit, ~~at least~~ only one of the clock leads at one time receiving a clock signal that controls ~~a~~ the state of the mode signal formed on the mode output lead.

21. (currently amended)The system of claim 20 in which the ~~first circuit includes functional circuitry, the first mode is a functional mode and the second~~ test mode is a by-pass mode.

22. (currently amended)The system of claim 20 in which the ~~second~~ selector circuit ~~is a die selector circuit that~~ includes ~~D-type flip-flops, AND gates, OR gates and delay elements~~ state machine circuits coupled to the pair of clock leads.

23. (currently amended)The system of claim 20 in which the ~~first and second~~ pair of clock leads are both capable of receiving and sending clock signals.

24. (currently amended)The system of claim 20 in which the ~~second~~ selector circuit includes a state machine circuit, and each of the clock leads is coupled to the state machine circuit through a

clock input buffer and is connected to the other clock lead through a clock output ~~buffers and a state machine~~ buffer.

25. (currently amended) The system of claim 20 in which the ~~second~~ selector circuit includes ~~third and fourth~~ another pair of clock leads separate from the ~~first~~ functional circuit and at least one of the four clock leads receives a clock signal that controls the mode signal.

26. (currently amended) The system of claim 20 in which the ~~second~~ selector circuit includes ~~third and fourth~~ another pair of clock leads separate from the ~~first~~ functional circuit, ~~clock input buffers, clock output buffers and a state machine~~ and each of the another pair of clock leads is coupled to the state machine circuit through a clock input buffer and is connected to the other clock lead through a clock output buffer.

27-34. (canceled)